WHAT IS CLAIMED IS:

1. A semiconductor device with a normal mode and a test mode as an operation mode, comprising:

an internal circuit executing a predetermined process in accordance with an input signal to provide an output signal in accordance with said predetermined process;

a delay circuit delaying said input signal by respective different delay times to output n (n: natural number) delay signals in said test mode; and

n comparison circuits provided corresponding to said n delay signals, respectively, each of said n comparison circuits providing a comparison result indicating which of a corresponding delay signal output and said output signal from said internal circuit is output earlier in said test mode.

2. The semiconductor device according to claim 1, wherein said delay circuit includes n electric lines sequenced in advance, each delaying said input signal by said different delay times, and

said n electric lines having n path lengths, respectively, sequentially increased in length in increments of a predetermined distance in an order from the first to n-th electric lines.

3. The semiconductor device according to claim 2, wherein each of said n comparison circuits includes a logic circuit providing a comparison determination signal based on a logic operation between said corresponding delay signal and said output signal in said test mode,

said semiconductor device further comprising:

a conversion circuit providing n comparison determination signals sequenced in advance, output from said n comparison circuits one by one in the order from the first to n-th comparison determination signals in said test mode ,

an output terminal providing said output signal to an external source in said normal mode, and

a path switch provided between said output terminal and said internal circuit for disconnecting a path of providing said output signal to said external source in said test mode,

wherein said n comparison determination signals from said comparison circuit are provided from said output terminal to said external source in the order from the first to n-th comparison determination signals in said test mode.

4. The semiconductor device according to claim 3, wherein said conversion circuit includes

n temporary storage circuits sequenced in advance, temporarily storing said n comparison determination signals respectively,

n shift circuits provided corresponding to said n temporary storage circuit, respectively, and

n switches provided between said n temporary storage circuits and said n shift circuits, respectively, wherein

each of said n shift circuits temporarily stores applied data, and a p-th (p: natural number of at least 2 and not more than n) shift circuit responds to a clock signal to output said applied data from a (p+1)th shift circuit to a (p-1)th shift circuit,

said n switches electrically connecting said n temporary storage circuits with said n shift circuits for a predetermined period after said n temporary storage circuits temporarily store said n comparison determination signals, respectively, and electrically disconnecting said n temporary storage circuits from said n shift circuits at an elapse of said predetermined period,

each of said n shift circuits receives said comparison determination signal from a corresponding temporary storage circuit for said predetermined period, and

said n comparison determination signals are output from the first shift circuit in order from the first to n-th comparison determination signals at an elapse of said predetermined period in response to said clock signal.

5. The semiconductor device according to claim 2, wherein each of said n electric lines has a path length modify section to delay said input signal for a predetermined time,

said path length modify section having

a first line electrically connecting first and second nodes located at respective sides of a predetermined site through a route of said predetermined site at a first distance,

a second line electrically connecting said first and second nodes at a second distance differing from said first distance,

said second line capable of being cut from outside said delay circuit,

said first distance being shorter than said second distance.

6. The semiconductor device according to claim 2, wherein each of said n electric lines has a path length modify section to delay said input signal for a predetermined time,

said path length modify section having

a first line electrically connecting first and second nodes located at respective sides of a predetermined site through a route of said predetermined site at a first distance,

second line electrically connecting said first and second nodes at a second distance differing from said first distance through a route above or below said first line,

said second line capable of being cut from outside said delay circuit,

said first distance being shorter than said second distance.

7. The semiconductor device according to claim 2, wherein each of said n comparison circuits includes a first logic circuit providing a comparison determination signal based on a logic operation between said corresponding delay signal and said output signal in said test mode,

said semiconductor device further comprising a determination circuit receiving n comparison determination signals sequenced in advance, output from said n comparison circuits in said test mode,

wherein said determination circuit includes a plurality of second

logic circuits to which are applied an arbitrary group of said n comparison determination signals in said test mode, each arbitrary group of said n comparison determination signals partially having different comparison determination signals from each other,

said each arbitrary group of n comparison determination signals including m(m: natural number smaller than n) sequential comparison determination signals among said n comparison determination signals, and

each of said plurality of second logic circuits providing a logic operation result of said m sequential comparison determination signals.

8. The semiconductor device according to claim 7, wherein said plurality of second logic circuits are selectively rendered active in accordance with a time required for said output signal from said internal circuit to be applied to said n comparison circuits.

9. The semiconductor device according to claim 7, further comprising:

an output terminal providing said output signal to an external source in said normal mode; and

a path switch provided between said output terminal and said internal circuit for disconnecting a path of providing said output signal to said external source in said test mode,

wherein said logic operation result from said determination circuit is output from said output terminal to said external source in said test mode.